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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/083,991	02/26/2002	Chia-Der Chang	TS01-660	5768

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EXAMINER
ISAAC, STANETTA D

ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 06/07/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/083,991	Applicant(s) CHANG ET AL.	
	Examiner Stanetta D. Isaac	Art Unit 2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-19 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-19 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

2. Claim1-19 rejected under 35 U.S.C. 102(e) as being anticipated by Jang et al Patent Number 6365523.

Jang discloses:

(See FIGS. 1-4; col. 6 lines 65-67; col. 7 lines 54-55; col. 8 lines 44-45; col. 9 lines 1-5,15-17, 55-59; col. 10 lines 63-65; col. 13 lines 50-52, 65-67; col.14 lines 1-2, 6-7, 16-17, 54-56)

1. A method of planarizing substrates having shallow trench isolation, comprising:

providing a substrate (10);

forming trenches in said substrate (11a-c);

depositing a layer of dielectric (14) on said substrate thereby filling said trenches with said dielectric;

forming a layer of resist (16a-e) on said layer of dielectric;

providing a polishing pad (32a-c) having a hardness of at least Shore "D" 5 ; and

removing said layer of resist and part of said layer of dielectric using said polishing pad and chemical mechanical polishing thereby leaving said trenches filled with trench dielectric and forming a planar surface.

2. The method of claim 1 wherein said substrate is a silicon wafer having devices formed therein.

3. The method of claim 1 wherein said dielectric is silicon dioxide deposited using high density plasma chemical vapor deposition. (col. 6 lines 65-67)

4. The method of claim 1 wherein said trenches are shallow trench isolation trenches. (col. 7 lines 54-55)

5. The method of claim 1 wherein said layer of resist is formed by spinning resist on said substrate followed by

baking said resist.

6. The method of claim 1 wherein said resist is photoresist.

7. The method of claim 6 wherein said photoresist is formed by spinning said photoresist on said substrate followed by baking said photoresist.

8. The method of claim 1 wherein said removing said layer of resist and part of said layer of dielectric removes that part of said layer of dielectric above said top surface of said substrate.

(13 lines 50-52, 65-67; col.14 lines 1-2, 6-7, 16-17, 54-56)

9. The method of claim 1 further comprising:

forming a layer of pad oxide on said substrate before said forming trenches in said substrate;

forming a layer of silicon nitride on said layer of pad oxide before said forming trenches in said substrate; and

forming trench openings in said layer of pad oxide and said layer of silicon nitride before said forming trenches in said substrate.

10. The method of claim 9 wherein said removing said layer

of resist and part of said layer of dielectric removes that part of said layer of dielectric above said layer of silicon nitride.

(See FIGS. 1-4; col. 6 lines 65-67; col. 7 lines 54-55; col. 8 lines 44-45; col. 9 lines 1-5,15-17, 55-59; col. 10 lines 63-65; col. 13 lines 50-52, 65-67; col.14 lines 1-2, 6-7, 16-17, 54-56)

11. A method of planarizing substrates having shallow trench isolation, comprising:

providing a substrate;

forming a dielectric base on said substrate;

forming trench openings in said dielectric base;

forming trenches in said substrate directly below said trench openings in said dielectric base;

depositing a layer of trench dielectric on said dielectric base thereby filling said trenches with said trench dielectric;

forming a layer of resist on said layer of trench dielectric;

providing a polishing pad having a hardness of at least Shore "D" 52; and

removing said layer of resist and part of said layer of trench dielectric using said polishing pad and chemical

mechanical polishing thereby leaving trench dielectric in said trenches and forming a planar surface.

12. The method of claim 11 wherein said substrate is a silicon substrate having devices formed therein.

13. The method of claim 11 wherein said trench dielectric is silicon dioxide deposited using high density plasma chemical vapor deposition.

14. The method of claim 11 wherein said dielectric base comprises a layer of pad oxide formed on said substrate and a layer of silicon nitride on said layer of pad oxide.
(col. 13 lines 50-52, 65-67; col.14 lines 1-2, 6-7, 16-17, 54-56)

15. The method of claim 14 wherein said removing said layer of resist and part of said layer of dielectric removes that part of said layer of dielectric above said layer of silicon nitride.

16. The method of claim 11 wherein said layer of resist is formed by spinning resist on said substrate followed by baking said resist.

17. The method of claim 11 wherein said resist is photoresist.

18. The method of claim 16 wherein said photoresist is formed by spinning said photoresist on said substrate followed by baking said photoresist.

19. The method of claim 11 wherein said removing said layer of resist and part of said layer of dielectric removes that part of said layer of dielectric above said dielectric base.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stanetta D. Isaac whose telephone number is 703-308-5871. The examiner can normally be reached on Monday-Friday 7:30am -5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Nebling can be reached on 703-308-3325. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-3432 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Stanetta Isaac
Patent Examiner
June 2, 2002

RICHARD BOOTH
PRIMARY EXAMINER